Our Reference: 2024.30 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Maimon
Serial Number: unknown
Filing Date: unknown
Examiner/Group Art Unit: unknown
Title: PROGRAMMABLE RESISTANCE MEMORY ELEMENT AND METHOD FOR MAKING SAME

CERTIFICATE OF MAILING BY EXPRESS MAIL UNDER 37 CFR 1.10

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed in this correspondence is:

1. new utility application
2. utility patent application transmittal
3. fee transmittal and copy thereof
4. return post card

I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office To Addressee" service under 37 CFR 1.10 in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on February 8, 2002 using Express Mail Label Number: ET932797078US.

Philip H. Schlazer
Reg. No. 42,127

DATE: February 8, 2002
Energy Conversion Devices, Inc.
2953 Waterview
Rochester Hills, MI 48309
Phone: (248) 293-0440 ext 6260

PROGRAMMABLE RESISTANCE MEMORY ELEMENT AND METHOD FOR MAKING SAME

RELATED APPLICATION INFORMATION

This application is a continuation-in-part of U.S. Patent Application Serial Number 09/891,157, filed on June 26, 2001.

FIELD OF THE INVENTION

The present invention relates generally to programmable resistance memory elements. More specifically, the present invention relates to a new structural relationship between the electrodes and the memory material which are integral parts of the memory element.

BACKGROUND OF THE INVENTION

Programmable resistance memory elements formed from materials that can be programmed to exhibit at least a high or low stable ohmic state are known in the art. Such programmable resistance elements may be programmed to a high resistance state to store, for example, a logic ZERO data bit. As well, they may be programmed to a low resistance state to store, for example, a logic ONE data bit.

One type of material that can be used as the memory material for programmable resistance elements is phase change material. Phase change materials may be programmed between a first structural state where the material is generally more amorphous

(less ordered) and a second structural state where the material is generally more crystalline (more ordered). The term "amorphous", as used herein, refers to a condition which is relatively structurally less ordered or more disordered than a single crystal and has a detectable characteristic, such as high electrical resistivity. The term "crystalline", as used herein, refers to a condition which is relatively structurally more ordered than amorphous and has lower electrical resistivity than the amorphous state.

The concept of utilizing electrically programmable phase change materials for electronic memory applications is disclosed, for example, in U.S. Patent Nos. 3,271,591 and 3,530,441, the contents of which are incorporated herein by reference. The early phase change materials described in the '591 and '441 Patents were based on changes in local structural order. The changes in structural order were typically accompanied by atomic migration of certain species within the material. Such atomic migration between the amorphous and crystalline states made programming energies relatively high.

The electrical energy required to produce a detectable change in resistance in these materials was typically in the range of about a microjoule. This amount of energy must be delivered to each of the memory elements in the solid state matrix of rows and columns of memory cells. Such high energy requirements translate into high current carrying requirements for the address lines and

for the cell isolation/address device associated with each discrete memory element.

The high energy requirements for programming the memory cells described in the '591 and '441 patents limited the use of these cells as a direct and universal replacement for present computer memory applications, such as tape, floppy disks, magnetic or optical hard disk drives, solid state disk flash, DRAM, SRAM, and socket flash memory. In particular, low programming energy is important when the EEPROMs are used for large-scale archival storage. Used in this manner, the EEPROMs would replace the mechanical hard drives (such as magnetic or optical hard drives) of present computer systems. One of the main reasons for this replacement of conventional mechanical hard drives with EEPROM "hard drives" would be to reduce the power consumption of the mechanical systems. In the case of lap-top computers, this is of particular interest because the mechanical hard disk drive is one of the largest power consumers therein. Therefore, it would be advantageous to reduce this power load, thereby substantially increasing the operating time of the computer per charge of the power cells. However, if the EEPROM replacement for hard drives has high programming energy requirements (and high power requirements), the power savings may be inconsequential or at best unsubstantial. Therefore, any EEPROM which is to be considered a universal memory requires low programming energy.

The programming energy requirements of a programmable

resistance memory element may be reduced in different ways. For example, the programming energies may be reduced by the appropriate selection of the composition of the memory material. An example of a phase change material having reduced energy requirements is described in U.S. Patent No. 5,166,758, the disclosure of which is incorporated by reference herein. Other examples of memory materials are provided in U.S. Patent Nos. 5,296,716, 5,414,271, 5,359,205, and 5,534,712, the disclosures of which are all hereby incorporated by reference herein.

The programming energy requirement may also be reduced through the appropriate modification of the electrical contacts used to deliver the programming energy to the memory material. For example, reduction in programming energy may be achieved by modifying the composition and/or shape and/or configuration (positioning relative to the memory material) of the electrical contacts. Examples of such "contact modification" are provided in U.S. Patent Nos. 5,341,328, 5,406,509, 5,534,711, 5,536,947, 5,687,112, 5,933,365, the disclosures of which are all hereby incorporated by reference herein. Examples are also provided in U.S. Patent Application Serial Nos. 09/276,273, 09/620,318, 09/677,957 and 09/891,157, the disclosures of which are all hereby incorporated by reference herein. The present invention is directed to novel structures of programmable resistance memory devices that may further reduce the programming energy requirements of such devices. The present invention is also

directed to methods for making these structures.

SUMMARY OF THE INVENTION

One aspect of the present invention is a programmable resistance memory element, comprising: a first dielectric material having a sidewall surface; a conductive layer formed over the sidewall surface; a second dielectric material formed over the conductive layer, wherein an edge of the conductive layer is exposed; a third dielectric material formed over the edge, the third dielectric material having a opening formed therethrough uncovering a portion of the edge; and a programmable resistance material disposed in the opening and in communication with the edge.

Another aspect of the present invention is a programmable resistance memory element, comprising: a first layer of a conductive material; a second layer of a programmable resistance material, wherein an edge of the first layer is adjacent to an edge of the second layer.

Another aspect of the present invention is a programmable resistance memory element, comprising: a layer of a conductive material; a trench or pore of programmable resistance memory material adjacent to an edge of the layer of conductive material.

Another aspect of the present invention a method of forming an opening in a layer of a first material of a semiconductor device: providing the layer of the first material; forming a

layer of a second material over the layer of the first material; forming a layer of a third material over the layer of the material; forming a sidewall surface in the layer of the third material; forming a sidewall spacer of a forth material on the sidewall surface; forming a layer of a fifth material over the sidewall spacer and an exposed portion of the layer of the second material; removing a portion of the fifth material to expose the sidewall spacer; removing the sidewall spacer; removing a portion of the layer of the second material exposing the layer of the first material; and removing a portion of the layer of the first material to form the opening.

Another aspect of the present invention is a method of forming an opening in a layer of a first material of a semiconductor device: providing the layer of the first material; forming a layer of a second material over the layer of the material; forming a sidewall surface in the layer of the second material; forming a sidewall spacer of a third material on the sidewall surface; forming a layer of a forth material over the sidewall spacer and an exposed portion of the layer of the first material; removing a portion of the forth material to expose the sidewall spacer; removing the sidewall spacer; and removing a portion of the layer of the first material to form the opening.

Another aspect of the present invention is a method of forming a programmable resistance memory element, comprising the steps of: providing a layer of a conductive material; forming a

layer of a first material over the layer of the conductive material; forming a layer of a second material over the layer of the first material; forming a layer of a third material over the layer of the material; forming a sidewall surface in the layer of the third material; forming a sidewall spacer of a forth material on the sidewall surface; forming a layer of a fifth material over the sidewall spacer and an exposed portion of the layer of the second material; removing a portion of the fifth material to expose the sidewall spacer; removing the sidewall spacer; removing a portion of the layer of the second material exposing the layer of the first material; removing a portion of the layer of the first material to form the opening; and depositing a programmable resistance material into the opening, the programmable resistance material in communication with the layer of the conductive material.

Another aspect of the present invention is a method of forming a programming resistance memory element, comprising the steps of: providing a layer of a conductive material; forming a layer of a first material over the layer of the conductive material; forming a layer of a second material over the layer of the material; forming a sidewall surface in the layer of the second material; forming a sidewall spacer of a third material on the sidewall surface; forming a layer of a forth material over the sidewall spacer and an exposed portion of the layer of the first material; removing a portion of the forth material to expose the

sidewall spacer; removing the sidewall spacer; removing a portion of the layer of the first material to form the opening; and depositing a programmable resistance material into the opening, the programmable resistance material in communication the layer of the conductive material.

It is noted that the two or more of the first, second, third, forth, and fifth materials may be the same material (or each may be a different material).

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a high-level diagram of a memory device of the present invention including a memory array and periphery circuitry formed on a substrate;

Figure 2A shows a high-level diagram of a memory array of the present invention;

Figure 2B is a schematic diagram of a memory array of the present invention;

Figure 3 is a schematic diagram of a memory cell incorporating a programmable resistance material;

Figures 4A through 18 shows a process for making an embodiment of the memory cell of the present invention;

Figure 19 shows an embodiment of the memory cell of the present invention;

Figure 20 shows a top view of the memory cell of the present invention;

Figures 21A through 21D show alternate process steps for making an embodiment of the present invention; and

Figures 22A through 22D show alternate process steps for making an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following paragraphs and in association with the accompanying figures, examples of memory devices formed according to embodiments of the invention are presented. Specific embodiments of memory elements and methods of making such memory elements are described below as they might be implemented for use in semiconductor memory circuits. In the interest of clarity, not all features of an actual implementation are described in this specification.

The present invention is directed to programmable resistance memory elements. The memory element comprises a volume of memory material which is programmable between a first resistance state and a second resistance state in response to an electrical signal. The memory element further comprises a means of delivering the electrical signal to the volume of memory material. Preferably, the means of delivering the electrical signal comprises a first and a second electrical contact, also referred to as first and second electrodes, which are in electrical communication with the volume of memory material. The electrical contacts or electrodes do not have to be in physical contact with the memory material.

(It is noted, that as used herein, the terminology "electrical contacts" and "electrodes" are synonymous and may be used interchangeably).

Turning now to the drawings, and referring initially to Figure 1, a memory device is illustrated and generally designated by a reference numeral 10. The memory device 10 is an integrated circuit memory formed on a semiconductor substrate 100. The memory device 10 includes a memory matrix or array 14 that includes a plurality of memory cells for storing data. The memory matrix 14 is coupled to periphery circuitry 16 by the plurality of control lines 18. The periphery circuitry 16 may include circuitry for addressing the memory cells contained within the memory array 14, along with circuitry for storing data in and retrieving data from the memory cells. The periphery circuitry 16 may also include other circuitry used for controlling or otherwise insuring the proper functioning of the memory device 10.

A top view of the memory array 14 is shown in Figure 2A. As can be seen, the memory array includes a plurality of memory cells 20 that are arranged in generally perpendicular rows and columns. As can be seen, the memory array 14 includes a plurality of memory cells 20 that are arranged in generally perpendicular rows and columns. The memory cells 20 in each row are coupled together by a respective wordline 22, and the memory cells 20 in each column are coupled together by a respective bitline 24.

A schematic diagram of the memory array 14 is shown in Figure 2B. As can be seen, each memory cell 20 includes a wordline node 26 that is coupled to a respective wordline 22, and each memory cell 20 includes a bitline node 28 that is coupled to a respective bitline 24. The conductive wordlines 22 and bitlines 24 are collectively referred to as address lines. These address lines are electrically coupled to the periphery circuitry 16 (shown in Figure 1) so that each of the memory cells 20 can be accessed for the storage and retrieval of information.

Figure 3 illustrates an exemplary memory cell 20 that may be used in the memory array 14. The memory cell 20 includes a memory element 30 which is coupled to an access device 32. The access device electrically isolates each memory element from all other memory elements in the array. In this embodiment, the memory element 30 is illustrated as a programmable resistive element, and the access device 32 is illustrated as a diode. The programmable resistive element may be made of a chalcogenide material, as will be more fully explained below. As illustrated in Figure 3, the memory element 30 is coupled to a wordline 22, and the access device 32 is coupled to a bitline 24. However, it should be understood that connections of the memory element 20 may be reversed without adversely affecting the operation of the memory array 14.

A structure of an exemplary memory cell 20 is illustrated in Figure 19, while a method for fabricating the memory cell 20 is

described with reference to Figures 4A-18. It should be understood that while the fabrication of only a single memory cell 20 is discussed below, a plurality of similar memory cells may be fabricated simultaneously. Although not illustrated, each memory cell is electrically isolated from other memory cells in the array in any suitable manner, such as by the addition of imbedded field oxide regions between each memory cell.

Referring first to Figure 4A, a semiconductor substrate 100 is provided. The substrate 100 may include the access devices as well as the bitlines and/or wordlines. A layer of dielectric material 110 is formed on top of the substrate 100. The layer 110 may be comprised of any suitable dielectric material, such as silicon nitride or silicon dioxide. The dielectric layer 110 may be formed in any suitable manner, such as by chemical vapor deposition (CVD). The dielectric layer 110 has a top surface 110T.

Referring to Figure 4A, an opening 120 (also referred as a "window") is formed through the dielectric layer 110 to expose a portion of the underlying substrate. Generally, the opening 120 may be any shape. For example, the opening 120 may be formed as a hole (such as a substantially circular or rectangular hole). Alternately, the opening 120 may be formed as a trench. The opening 120 includes the sidewall surface 120S about the periphery of the opening and the bottom surface 120B. The opening 120 is preferably a substantially circular hole as shown

in Figure 4B.

Any suitable method of forming the opening 120 may be used. For example, using standard photolithographic techniques, a hard mask (not shown) may be deposited on top of the dielectric layer 110 and patterned in the size and shape of the resulting opening 120. Hence, the opening 120 may be sized at the photolithographic limit.

As shown in Figure 5, a layer 130 of a conductive material is deposited on top of the structure shown in Figures 4A and 4B. The layer 130 of conductive material is deposited on top surfaces 110T of the dielectric region 110 as well as on the sidewall surface 120S and on the bottom surface 120B of opening 120. Preferably, the deposition of the layer 130 is a substantially conformal deposition. Hence, the layer 130 has a top portion 130T, a sidewall layer portion 130S, and a bottom layer portion 130B.

The conductive material used for layer 130 may be any conductive material. Examples of materials which may be used for layer 130 are include, but are not limited to, n-type doped polysilicon, p-type doped polysilicon, p-type doped silicon carbon alloys and/or compounds, n-type doped silicon carbon alloys and/or compounds, titanium-tungsten, tungsten, tungsten silicide, molybdenum, and titanium nitride. Other examples include titanium carbon-nitride, titanium aluminum-nitride, titanium silicon-nitride, and carbon.

Referring to Figure 6, a layer of dielectric material 140

(such as silicon dioxide) may then be deposited on top of the layer 130. Preferably, the dielectric layer 140 fills the remaining portion of opening 120 and is deposited above the top surfaces 110T. The structure shown in Figure 6 may then be chemically mechanically polished (CMP) or dry etched so as to planarize the top surface, thereby removing the top surface portion 130T of the layer 130 and forming the bottom electrode 134 as shown in Figure 7A (cross-sectional view parallel to the x-z plane) and in Figure 7B (three-dimensional view). The bottom electrode 134 is in the form of a cylindrical, cup-shaped conductive liner 134. The bottom electrode 134 has a top edge portion 136 which is in the shape of an annulus. The bottom electrode 134 has a sidewall layer portion 134S and a bottom layer portion 134B. The bottom electrode has a thickness "W1" which is defined by the thickness of the conformal deposition of conductive layer 130 shown in Figure 5. Preferably, the thickness W1 is smaller than that which could be achieved by standard photolithography. That is, the thickness W1 is preferably less than the photolithographic limit. In one embodiment of the present invention, the thickness W1 is preferably less than about 500 Angstroms and, more preferably, less than about 300 Angstroms.

In the example shown in Figures 7A and 7B, the bottom electrode 134 is cylindrically shaped and the exposed edge 136 forms an annularly shaped contact surface. As discussed above,

the opening 120 (shown in Figures 4A and 4B) may also be formed as a trench. In this case, the resulting bottom electrode would be a conductive sidewall liner that is U-shaped, having a bottom surface and two sidewall surfaces. The resulting exposed edge portion of the U-shaped conductive liner would be two linear contact surfaces. In an alternate embodiment of the invention, the bottom electrode may be formed as a conductive spacer rather than as a conductive liner.

Figure 7C shows a top view of the bottom electrode 134 showing the top edge 136 and dielectric 140. Figure 7A is the cross-sectional view through taken from line 142-142 of Figure 7C. Figure 7D is the cross-sectional view taken from line 144-144 of Figure 7C.

Referring to Figure 8, a layer 150 is deposited over the top surface of the structure shown in Figure 7D (again, this is the cross-sectional view taken from line 144-144 of Figure 7C). Preferably, the layer 150 is formed of a dielectric material. Any dielectric material may be used (such as an oxide or a nitride). More preferably, the layer 150 is formed from an oxide. Most preferably, the layer 150 is formed from silicon dioxide from a TEOS source. The layer 150 may be deposited by any suitable manner such as by chemical vapor deposition or by physical vapor deposition.

A layer 160 is then deposited over the oxide layer 150. Preferably, the layer 160 is formed from a nitride (such as a

silicon nitride). However, in another embodiment of the invention is possible to form the layer 160 from any other dielectric (such as an oxide). In yet other embodiments of the invention, it is possible that layer 160 be formed from a semi-conductor (such a polysilicon) or a conductor (such as a metal).

A layer 170 is then deposited over the nitride layer 160 to form the structure shown in Figure 8. The layer 170 is preferably formed from an oxide (such as silicon dioxide from a TEOS source). However, in another embodiment of the invention is possible for form layer 170 from any other dielectric (such as a nitride). In yet other embodiments of the invention, it is possible that layer 170 be formed from a semi-conductor (such a polysilicon) or a conductor (such as a metal).

The oxide layer 170 is then patterned selective to the nitride layer 160 to form the sidewall surface 170S as shown in Figure 9A. The position of the sidewall surface 170S relative to the edge portion 136 of the conductive liner 134 is shown in Figure 9B which is a top view of the structure from Figure 9A.

Referring to Figure 10, a layer 180 then deposited over the structure shown in Figure 9A. Preferably, the layer 180 is formed from a polysilicon. As shown, the polysilicon 180 is deposited over the top surface and sidewall surface 170S of the second oxide layer 170. The layer 180 is also deposited over an exposed portion of the nitride layer 160. Preferably, the deposition of the polysilicon layer 180 is a substantially conformal deposition.

In other embodiments of the invention, it is possible that the layer 180 be formed of another type of material. For example, layer 180 may be formed of a dielectric material (such as an oxide or nitride). In yet other embodiments of the invention, it is even possible that the layer 180 be formed of a conductor (such as a metal).

Referring to Figure 11, the horizontally disposed portions of the polysilicon layer 180 are then removed preferably by an anisotropic etch of the polysilicon layer (the etch used is preferably selective to the TEOS oxide 170 and the nitride 160). The anisotropic etch leaves the polysilicon sidewall spacer 185.

Referring to Figure 12, a layer 190 is then deposited over the structure shown in Figure 11 to form the structure shown in Figure 12. The layer 190 is preferably formed of the same material as the layer 170 which, in the embodiment shown, is an oxide (such as silicon dioxide from a TEOS source). However, like layer 170, it is possible (in other embodiments of the invention) to form the layer 190 from another type of dielectric (such as a nitride), from a semi-conductor or from a conductor. The layer 190 is deposited over the top surface of layer 170, over the sidewall spacer 185 and over an exposed portion of the nitride layer 160. As shown in Figure 12, oxide material 170 and oxide material 190 are present on opposite sides of the sidewall spacer 185.

The structure shown in Figure 12 is then chemically

mechanically polished to remove a portion of the oxide layer 190 and to expose the top surface of the polysilicon spacer 185 and form the structure shown in Figure 13. The structure shown in Figure 13 may, optionally, be subjected to a partial etch of both of the top oxide layers 170, 190 (to reduce the thickness of these oxide layers). Referring to Figure 14, the polysilicon spacer 185 is then removed by being etched selective to the TEOS oxide layers 170, 190. This forms the trench or slot-like opening 200 between the oxide layers 170 and 190. The opening 200 exposes a portion of the nitride layer 160.

The nitride layer 160 is then etched selective to the oxide thereby extending the opening 200 through the nitride layer to expose the top surface of oxide layer 150 as shown in Figure 15. The oxide layers 150, 170 and 190 are then etched selective to the nitride layer 160 to form the structure shown in Figure 16. (Optionally, prior to this last oxide etch, the oxide layers 170, 190 may be chemically mechanically polished to reduce the thickness of these layers).

As shown in Figure 16, the oxide etch removes the oxide layers 170, 190 and also extends the opening 200 through the oxide layer 150 so as to expose or uncover a portion of the top edge 136 of the bottom electrode 134. Referring to Figure 17, the nitride layer 160 is then removed by being etched selective to the oxide layer 150. The nitride etch may be performed using a hot phosphoric acid.

Referring to Figure 17, it is noted that the opening 200 is in the form of a narrow trench or slot having a bottom surface 202. The opening 200 has a width "W2" (a lateral dimension of the opening) which is very small. In one embodiment of the invention, the width "W2" is less than the photolithographic limit. The width "W2" is preferably less than about 500 Angstroms and, is more preferably less than about 300 Angstroms.

Referring to Figure 18, a layer 210 of programmable resistance material is deposited over the oxide layer 150 and into the opening 200. The programmable resistance material is thus adjacent to (and preferably makes contact with) the exposed portion of the top edge of the bottom electrode 134. The programmable resistance material is in electrical communication with the bottom electrode 134. Substantially all electrical communication between the bottom electrode 134 and the programmable resistance material is preferably through the exposed portion of the top edge 136 of the bottom electrode 134. A layer 220 of conductive material is then deposited over the layer 210 of programmable resistance material. The conductive layer 220 forms the top electrode of the memory device. A three-dimensional view of the memory device is shown in Figure 19.

It is noted that the memory device shown in Figures 18 and 19 may be formed using alternate processing steps. An example of alternate process steps is shown in Figures 21A through 21D. Figure 21A shows the cross-section of the memory device from

Figure 11. Referring to Figure 21B, it is possible at this stage of the process to remove the oxide layer 170 to form the structure shown in Figure 21B. That is, the oxide layer 170 is etched selective to the polysilicon spacer 185 and selective to the underlying nitride layer 160. An oxide layer 190 is then deposited over the exposed portion of nitride layer 160 and over the polysilicon sidewall spacer 185 to form the structure shown in Figure 21C. The structure shown in Figure 21C may then be chemically mechanically polished to remove a portion of the oxide layer 190 and to expose the top surface of the polysilicon spacer and form the structure shown in Figure 21D. The structure shown in Figure 21D is the same as the structure shown in Figure 13 except that oxide material 190 (of Figure 21D replaces oxide material 170 of Figure 13). The oxide material 190 is present on opposite sides of the sidewall spacer 185 and the sidewall spacer 185 may be removed to form an opening in the oxide material 190. Hence, the processing steps shown in Figures 21A-D may be used to replace the processing steps shown in Figures 11-13. (The CMP step of Figure 21D may be easier to do than the CMP step of Figure 13).

Another example of using alternate processing steps is shown in Figures 22A - 22D. Figure 22A shows a cross-sectional view of the memory device from Figure 15. Figure 22A shows the oxide layers 170, 190, nitride layer 160 and the trench-like opening 200 that extends through oxide layers 170, 190 as well as nitride

layer 160. The opening 200 extends to the top surface of oxide layer 150. Referring to Figure 22B, the oxide layers 170 and 190 are removed by being etched selective to the underlying nitride layer 160. Oxide layer 150 is also etched at the same time as the oxide layers 170, 190. Referring to Figure 22B, it is seen that oxide layer 150 is etched to form a recess in the oxide layer 150 that does not go all the way through the oxide layer 150 (the recess may go through about two-thirds of the oxide layer 150). Hence, the opening 200 is extended only partially through the oxide layer 150. Referring to Figure 22C the nitride layer 160 is then removed, preferably by being etched selective to the underlying oxide. Referring to Figure 22D, the entire oxide layer 150 is then etched to remove the remaining portion of the oxide material within the opening 200 thereby extending the opening all the way to the top surface of the bottom electrode 200. This last oxide etch also decreases the thickness of the remaining portion of the oxide layer 150. It is noted that the structure shown in Figure 22D is similar to that shown in Figure 17. The processing steps shown in Figures 22A-D thus replaces the processing steps shown in Figures 15-17.

Referring again to Figure 12, it is again noted that in one embodiment of the invention, layers 150, 170 and 190 are preferably oxides (such as a silicon dioxide); the spacer 185 is preferably formed of polysilicon; and layer 160 is preferably formed of a nitride (such as silicon nitride). However, it is

again noted that other materials may be used for each of the layers. For example the layer 150 may be formed of any other dielectric (such as a nitride). Generally, the layers 160, 170, 185 and 190 may be formed from a dielectric (such as oxide or nitride), semi-conductor (such as polysilicon), or conductor (such as a metal). The material selected for each layer is preferably chosen to provide the proper selectivity during the etching process steps as will be recognized by persons of ordinary skill in the art.

In yet other embodiments of the invention, it is possible to form the memory device without the use of the layer 160 (shown in Figures 8-16, 21A-D, 22A-B). For example, referring to Figure 12, the layers 170, 185 and 190 may be formed directly over layer 150 without the need to first deposit layer 160 over layer 150. The layer 160 may be removed from the sequence of processing steps by appropriately selecting the materials used for the remaining layers 150, 170, 185 and 190. As noted above, the material used for each layer is preferably chosen to provide the proper selectivity during the etching process steps. As an example, it is possible that in one embodiment of the invention, layer 150 is chosen to be an oxide, layers 170 and 190 chosen to be a nitride, and layer 185 chosen to be polysilicon. As another example, it is possible that in another embodiment, layer 150 be chosen to be a nitride, layers 170 and 190 chosen to be an oxide, and layer 185 chosen to be polysilicon.

Referring to Figures 18 and 19, it is noted that the memory structure of the present invention provides for a very small total area of contact between the bottom electrode 134 and the programmable resistance memory material 150. Preferably, substantially all electrical communication between the bottom electrode 134 and the memory material 150 is through that portion of the upper edge 136 that is adjacent to (or actually makes contact with) the bottom surface 202 of the opening 200.

The two areas of contact "A1" and "A2" between the memory material and the bottom electrode may be seen in Figure 20 which shows a top view of the slot 200 in relation to the edge 136 of the bottom electrode 134. As noted above, the thickness "W1" of the upper edge 136 may be less than or equal to about 300 Angstroms while the width "W2" of the opening 200 may be less than or equal to about 300 Angstroms. Hence, the surface area of each area of contact A1 and A2 may be less than or equal to about 90,000 square Angstroms.

It is noted that in the embodiment of the invention shown in Figure 19, the opening 200 is in the form of a narrow slot. However, in an alternate embodiment of the invention, the opening 200 may be in the form of a hole or pore. This will also result in a small area of contact between the bottom electrode and the programmable resistance material deposited into the hole.

In addition, in an alternate embodiment of the present invention is also possible to form a layer of programmable

resistance memory material and position the layer of memory material so that only an edge of the memory material is adjacent to the edge 136 of the bottom electrode. Hence, substantially all electrical communication between the bottom electrode 134 and the memory material would be through the portion of the edge of the electrode and the portion of the edge of the memory material that are adjacent (or in actual contact). This "edge-to-edge" type of structure also provides for a small area of contact between the memory material and bottom electrode. Preferably, the edge of the programmable resistance material is positioned transverse to edge of the bottom electrode.

It is further noted that one or more additional layers may be disposed between the bottom electrode and the programmable resistance material. For example, a barrier layer may, optionally, be formed between the top edge of the bottom electrode and the programmable resistance material. Barrier layer materials may be chosen to increase the conductivity between the bottom electrode and the memory material, and/or improve the adhesion between the bottom electrode and the memory material, and/or to prevent the electromigration of the electrical contact material into the memory material. Examples of certain barrier layer materials include, but are not limited to, titanium silicide, cobalt silicide and tungsten silicide.

The memory elements of the present invention may be electrically coupled to isolation/selection devices and to

addressing lines in order to form a memory array. The isolation/addressing devices permit each discrete memory cell to be read and written to without interfering with information stored in adjacent or remote memory cells of the array. Generally, the present invention is not limited to the use of any specific type of isolation/addressing device. Examples of isolation/addressing devices include field-effect transistors, bipolar junction transistors, and diodes. Examples of field-effect transistors include JFET and MOSFET. Examples of MOSFET include NMOS transistors and PMOS transistors. Furthermore NMOS and PMOS may even be formed on the same chip for CMOS technologies.

Hence, associated with each memory element of a memory array structure is isolation/addressing device which serves as an isolation/addressing device for that memory element thereby enabling that cell to be read and written without interfering with information stored in other adjacent or remote memory elements of the array.

The programmable resistance material may be programmed to at least first resistance state and a second resistance state. The programmable resistance material is preferably programmed by electrical signals (such as currents). In one embodiment, the memory material is programmable to two resistance states so that each of the memory elements is capable of storing a single bit of information. In another embodiment, the memory material is programmable to at least three resistance states so that each of

the memory elements is capable of storing more than one bit of information. In yet another embodiment, the memory material is programmable to at least four resistance states so that each of the memory elements is capable of storing at least two bits of information. Hence, the memory materials may have a range of resistance values providing for the gray scale storage of multiple bits of information.

The programmable resistance materials may be directly overwritable so that they can be programmed from any of their resistance states to any other of their resistance states without first having to be set to a starting state. Preferably, the same programming pulse or pulses may be used to program the memory material to a specific resistance state regardless of its previous resistance state. (For example, the same current pulse or pulses may be used to program the material to its high resistance state regardless of its previous state). An example of a method of programming the memory element is provided in U.S. Patent No. 6,075,719, the disclosure of which is incorporated by reference herein.

The memory material may be a phase change material. The phase-change materials may be any phase change memory material known in the art. Preferably, the phase change materials are capable of exhibiting a first order phase transition. Examples of materials are described in U.S. Patent Nos. 5,166,758, 5,296,716, 5,414,271, 5,359,205, 5,341,328, 5,536,947, 5,534,712, 5,687,112,

and 5,825,046 the disclosures of which are all incorporated by reference herein.

The phase change materials may be formed from a plurality of atomic elements. Preferably, the memory material includes at least one chalcogen element. The chalcogen element may be chosen from the group consisting of Te, Se, and mixtures or alloys thereof. The memory material may further include at least one element selected from the group consisting of Ge, Sb, Bi, Pb, Sn, As, S, Si, P, O, and mixtures or alloys thereof. In one embodiment, the memory material comprises the elements Te, Ge and Sb. In another embodiment, the memory material consists essentially of Te, Ge and Sb. An example of a memory material which may be used is $Te_2Ge_2Sb_5$.

The memory material may include at least one transition metal element. The term "transition metal" as used herein includes elements 21 to 30, 39 to 48, 57 and 72 to 80. Preferably, the one or more transition metal elements are selected from the group consisting of Cr, Fe, Ni, Nb, Pd, Pt and mixtures or alloys thereof. The memory materials which include transition metals may be elementally modified forms of the memory materials in the Te-Ge-Sb ternary system. This elemental modification may be achieved by the incorporation of transition metals into the basic Te-Ge-Sb ternary system, with or without an additional chalcogen element, such as Se.

A first example of an elementally modified memory material is

a phase-change memory material which includes Te, Ge, Sb and a transition metal, in the ratio $(Te_aGe_bSb_{100-(a+b)})_cTM_{100-c}$ where the subscripts are in atomic percentages which total 100% of the constituent elements, wherein TM is one or more transition metals, a and b are as set forth herein above for the basic Te--Ge--Sb ternary system and c is between about 90% and about 99.99%. Preferably, the transition metal may include Cr, Fe, Ni, Nb, Pd, Pt and mixtures or alloys thereof.

A second example of an elementally modified memory material is a phase-change memory material which includes Te, Ge, Sb, Se and a transition metal, in the ratio $(Te_aGe_bSb_{100-(a+b)})_cTM_dSe_{100-(c+d)}$ where the subscripts are in atomic percentages which total 100% of the constituent elements, TM is one or more transition metals, a and b are as set forth hereinabove for the basic Te-Ge-Sb ternary system, c is between about 90% and 99.5% and d is between about 0.01% and 10%. Preferably, the transition metal may include Cr, Fe, Ni, Pd, Pt, Nb, and mixtures or alloys thereof.

It is to be understood that the disclosure set forth herein is presented in the form of detailed embodiments described for the purpose of making a full and complete disclosure of the present invention, and that such details are not to be interpreted as limiting the true scope of this invention as set forth and defined in the appended claims.